1. (Currently amended) An integrated circuit (IC) ~~providing identical functionality and performance in two selectable fabrication options, wherein~~ comprising:

a first selectable fabrication option ~~comprises~~ comprised of a user configurable memory circuit; and

a second selectable fabrication option comprises comprised of a hard-wired circuit in lieu of said user configurable ~~circuit.~~ memory circuit;

wherein, the IC functionality and performance is substantially identical for a given configuration utilizing the first or second fabrication options.

2. (Original) The IC of claim 1, wherein said first selectable option comprises a configurable Random Access Memory (RAM) module.

3. (Original) The IC of claim 1, wherein said second selectable option comprises a Read Only Memory (ROM) module.

4. (Original) The IC of claim 1, further comprising:

an input, said input received at an input-pad; and

an output, said output generated at an output-pad; and

an input to output signal propagation delay, said delay substantially identical between said first and said second selectable fabrication options.

5. (Currently amended) The ~~method~~ IC of claim 1, wherein providing said second selectable hard-wire circuit comprises at least one custom mask, said at least one mask facilitating:

a power-bus connection to replace a logic one in said configurable memory circuit; and

a ground-bus connection to replace a logic zero in said configurable memory circuit.

6. (Original) The IC of claim 2, wherein said RAM element is selected from one of volatile and non-volatile memory elements.

7. (Original) The circuit of claim 2, wherein said RAM element is selected from one of fuse links, anti-fuse capacitors, SRAM cells, DRAM cells, metal optional links, EPROM cells, EEPROM cells, flash cells, ferro-electric elements, optical elements, electro-chemical elements and magnetic elements.

8. (Currently amended) A programmable logic device (PLD) comprising two selectable memory construction options to control logic circuits, wherein:

a first selectable option comprises a random access memory (RAM) construction; and

a second selectable option comprises a hard-wire read only memory (ROM) ~~construction.~~ construction;

wherein, the logic circuits construction comprises one or more masking patterns that are invariant to the memory construction options.

9. (Original) The device of claim 8, wherein said first selectable option comprises a configuration circuit to configure said RAM.

10. (Original) The device of claim 8, wherein said second selectable option comprises

mapping one of said first selectable option RAM bit patterns to a hard-wire ROM pattern.

11. (Original) The device of claim 8, further comprising:

an input, said input received at an input-pad; and

an output, said output generated at an output-pad; and

an input to output signal propagation delay, said delay substantially identical between said RAM and said ROM logic control options.

12. (Original) The device of claim 8, wherein said RAM element is selected from one of volatile and non-volatile memory elements.

13. (Original) The device of claim 8, wherein said RAM element is selected from one of fuse links, anti-fuse capacitors, SRAM cells, DRAM cells, metal optional links, EPROM cells, EEPROM cells, flash cells, ferro-electric elements, optical elements, electro-chemical elements and magnetic elements.

14. (Original) The device of claim 8, further comprising a pass-gate logic element, said logic element providing a programmable means of electrically connecting or disconnecting two nodes.

15. (Original) The device of claim 14, wherein said programmable means in said first selectable option comprises configuring a RAM bit, said RAM bit generating:

a logic one output to connect said two nodes; and

a logic zero output to disconnect said two nodes.

16. (Original) The device of claim 14, wherein said programmable means in said second selectable option comprises hard-wiring a ROM bit, said ROM bit providing:

a hard-wire to power-bus to connect said two nodes; and

a hard-wire to ground-bus to disconnect said two nodes.

17. (Currently amended) A configurable pass-gate logic element ~~for a PLD, said pass-gate electrically coupling two nodes, said configuration achieved by a memory element, said memory element comprising two selectable construction options, wherein~~ to electrically couple two nodes in a programmable logic device (PLD), comprising:

a configuration circuit to configure the pass-gate, said configuration achieved by a memory element in the configuration circuit, wherein the memory element construction comprises:

a first selectable option ~~constitutes~~ comprising a random access memory (RAM) construction; and

a second selectable option ~~constitutes~~ comprising a hard-wire read only memory (ROM) ~~construction.~~ construction;

wherein, the pass-gate logic element construction comprises one or more masking patterns that are invariant to the memory construction options.

18. (Original) The element of claim 17, further comprised of a first node to a second node signal propagation delay, said delay substantially identical between said first and said second selectable memory construction options.

19. (Original) The element of claim 17, wherein constructing said second selectable hard-wire ROM comprises at least one custom mask, said at least one mask facilitating:

a power-bus ROM connection to replace a logic one in said RAM element; and

a ground-bus ROM connection to replace a logic zero in said RAM element.

20. (Original) The element of claim 17, wherein said RAM element is selected from one of fuse links, anti-fuse capacitors, SRAM cells, DRAM cells, metal optional links, EPROM cells, EEPROM cells, flash cells, ferro-electric elements, optical elements, electro-chemical elements and magnetic elements.